EXHIBIT 9

FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

ACQIS LLC, *Plaintiff*, v. SAMSUNG ELECTRONICS CO., LTD. and SAMSUNG ELECTRONICS AMERICA, INC., *Defendants*.	§ § § § § § § § § § §	Case No. 2:20-cv-00295-JRG

CLAIM CONSTRUCTION MEMORANDUM OPINION AND ORDER

Before the Court is the opening claim construction brief of ACQIS LLC ("Plaintiff") (Dkt. No. 65, filed on July 8, 2021),[1] Samsung Electronics Co., Ltd.'s and Samsung Electronics America, Inc.'s (collectively "Defendants") response (Dkt. No. 69, filed on July 27, 2021), and Plaintiff's reply (Dkt. No. 71, filed on August 3, 2021). The Court held a hearing on the issues of claim construction and claim definiteness on August 23, 2021. Having considered the arguments and evidence presented by the parties at the hearing and in their briefing, the Court issues this Order.

[1] Citations to the parties' filings are to the filing's number in the docket (Dkt. No.) and pin cites are to the page numbers assigned through ECF.

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I. BACKGROUND

Plaintiff alleges infringement of five U.S. Patents: No. 8,977,797 (the "'797 Patent"), No. 9,529,768 (the "'768 Patent"), No. 9,703,750 ("'750 Patent"), No. RE44,654 ("'654 Patent"), and No. RE45,140 ("'140 Patent") (collectively, the "Asserted Patents").

A. The '797, '768, and '750 Patents

The '797, '768, and '750 Patents are related. The '750 Patent issued from an application that is a continuation of the '768 Patent's application. The '768 Patent issued from an application that is a continuation of an application that is a continuation of the '797 Patent's application. Each of the '797, '768, and '750 Patents list an earliest priority claim to an application filed on May 14, 1999.

The abstracts of the '797, '768, and '750 Patents are identical and provide:

> A computer system for multi-processing purposes. The computer system has a console comprising a first coupling site and a second coupling site. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to a connector. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, and a mass storage device coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system.

Claim 7 of the '797 Patent, an exemplary asserted method claim, recites as follows (with terms in dispute emphasized):

> 7. A method of improving computer storage data throughput, comprising:
> connecting a Central Processing Unit (CPU) directly to a peripheral bridge on a printed circuit board of a computer system,
> connecting a Low Voltage Differential Signal (LVDS) channel directly to the peripheral bridge on the printed circuit board, the LVDS channel comprising two unidirectional, serial channels that transmit data in opposite directions;
> increasing data throughput of the serial channels by providing each channel with multiple pairs of differential signal lines;

conveying encoded address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in serial form over the serial channels to preserve the PCI bus transaction;
coupling the peripheral bridge to a mass storage device through the LVDS channel; and
applying power to the computer system.

B. The '654 and '140 Patents

The '654 and '140 Patents are related. The '140 Patent issued from an application that is a continuation of the '654 Patent's application. Each of the '654 and '140 Patents list an earliest priority claim to an application filed on May 14, 1999.

The abstracts of the '654 and '140 Patents are identical and provide:

> A security method for an attached computer module in a computer system. The security method reads a security identification number in an attached computer module and compares it to a security identification number in a console, which houses the attached computer module. Based upon a relationship between these numbers, a security status is selected. The security status determines the security level of operating the computer system.

Claim 30 of the '140 Patent, an exemplary asserted method claim, recites as follows (with terms in dispute emphasized):

> 30. A method of improving performance of a computer, comprising:
> obtaining an integrated Central Processing Unit (CPU) with a graphics controller in a single chip;
> connecting a Low Voltage Differential Signal (LVDS) channel directly to the integrated CPU and graphics controller, wherein the LVDS channel comprises two unidirectional, serial bit channels that transmit data in opposite directions;
> ***conveying serially encoded address and data of a Peripheral Component Interconnect (PCI) bus transaction*** through the LVDS channel;
> connecting a Differential Signal channel directly to the integrated CPU and graphics controller to output video data; and
> connecting memory directly to the integrated CPU and graphics controller.

C. Previous Litigation of Related Patents

Terms related to the terms in dispute here have previously been construed in patents related to Asserted Patents. Specifically, claim-construction disputes related to those presented here were

addressed in the following opinions: (1) *ACQIS LLC v. Alcatel-Lucent USA Inc. et al.*, No. 6:13-CV-638, 2015 U.S. Dist. LEXIS 48339 (E.D. Tex. Apr. 13, 2015) ("*Alcatel Markman*"), (2) *ACQIS, LLC v. EMC Corp.*, Civil Action No. 14-cv-13560, 2017 U.S. Dist. LEXIS 202160 (D. Mass. Dec. 8, 2017) ("*EMC Markman*"), and (3) *ACQIS, LLC v. EMC Corp.*, Civil Action No. 14-cv-13560-ADB, 2021 U.S. Dist. LEXIS 55945 (D. Mass. Feb. 19, 2021) ("*EMC Summary Judgment*"). The *Alcatel Markman* included a case with EMC Corp. (No. 6:13-cv-639) which was transferred to the District of Massachusetts. *EMC Markman*, 2017 U.S. Dist. LEXIS 202160, at *3–4. In this Order, the Court collectively refers to the Eastern District of Texas and District of Massachusetts cases with EMC Corp. as the "EMC Case."

As relevant to the issues before the Court here, the *Alcatel Markman* addressed the meaning of "Peripheral Component Interconnect (PCI) bus transaction" in, amongst others, U.S. Patent Nos. 8,041,873 and RE44,468.[2] Plaintiff there proposed a construction of "digital command, address, and data information, in accordance with the PCI standard, for communication with an interconnected peripheral component." *Alcatel Markman*, 2015 U.S. Dist. LEXIS 48339, at *12. The defendants there proposed "signals communicated over a PCI bus." *Id*. The Court resolved the dispute as follows:

> As for the proper construction, the parties agree that "PCI" refers to an industry standard. ACQIS cites a PCI Local Bus Specification to support its proposed construction involving digital command, address, and data information. … . Although ***a PCI bus transaction must include all information required by the PCI standard***, ***ACQIS's extrinsic evidence does not clearly define a "transaction" as digital command, address, and data information***. Accordingly, the Court construes "PCI bus … transaction" as "**information, in accordance with the PCI standard, for communication with an interconnected peripheral component.**"

[2] The '797, '768, and '750 Patents are related to U.S. Patent No. 8,041,873 through a series of continuation applications. '750 Patent, at [63] Related U.S. Application Data. Likewise, the '654 and '140 Patents are related to U.S. Patent No. RE44,468 through a series of continuation applications. '140 Patent, at [63] Related U.S. Application Data.

Id. at *14–15 (bold emphasis in original, bold-italic emphasis added).

The *EMC Markman* revisited the construction of "Peripheral Component Interconnect (PCI) bus transaction" set forth in the *Alcatel Markman*. Plaintiff there proposed a construction of "information, in accordance with the PCI Standard, for communicating with an interconnected peripheral component." *EMC Markman*, 2017 U.S. Dist. LEXIS 202160, at *9. The defendant there proposed "a transaction, as defined by the industry standard PCI Local Bus Specification involving a PCI bus." *Id*. The court noted the "central dispute remaining is whether the term requires the presence of a PCI bus," *id*. at *9–10, and held:

> The Court agrees with Judge Davis's [*Alcatel Markman*] interpretation …
>
> Moreover, the parties agree that "PCI bus transaction" incorporates the industry standard PCI Local Bus Specification. As Judge Davis noted, "***a PCI bus transaction must include all information required by the PCI standard***," but the PCI Local Bus Specification does not define such transactions by the presence of a PCI bus. …
>
> Accordingly, given Judge Davis's construction and the discussion above, the Court construes "Peripheral Component Interconnect (PCI) bus transaction" to mean "**a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component**."

Id. at *11–15 (bold emphasis in original, bold-italic emphasis added).

The *EMC Summary Judgment* reiterated the construction of "Peripheral Component Interconnect (PCI) bus transaction." The parties there disputed whether this term requires every element of the PCI Local Bus Specification. *EMC Summary Judgment*, 2021 U.S. Dist. LEXIS 55945, at *10–11. The *EMC Summary Judgment* court explained:

> During claim construction before Judge Davis, the parties agreed to construe the term "PCI bus transaction" according to the [PCI Local Bus] Specification. …. Judge Davis noted that "a PCI bus transaction must include all information required by the PCI standard." … Subsequently, in connection with this Court's Markman proceeding, the parties once again agreed to construe the term "PCI bus transaction" according to the [PCI Local Bus] Specification. … . Although ACQIS argued strenuously and successfully that a PCI bus was not

> required in a PCI bus transaction, ACQIS never sought to disavow the elements of the [PCI Local Bus] Specification pertaining to a physical bus. …
>
> ACQIS had ample opportunity to argue for a modified definition of the Specification during either court's claim construction proceedings, but chose not to do so. Judge Davis construed a PCI transaction as "information, in accordance with the PCI standard." … Then, in connection with this Court's claim construction, ACQIS agreed with EMC to use the relevant industry standard, the [PCI Local Bus] Specification. … ***There is no need to now construe a readily understandable term that ACQIS itself thought clear when offering proposed constructions of related terms and the Court will not do so***. …
>
> The Court rejects ACQIS's proffered modification of the claim term "PCI bus transaction" to narrow the application and meaning of the Specification. Accordingly, because the accused products do not contain the limitations set forth in the asserted claims, which recite a PCI bus transaction with reference to the [PCI Local Bus] Specification, the Court concludes that there is no infringement and summary judgment is appropriate.

Id. at *12–15 (emphasis added).

II. LEGAL PRINCIPLES

A. Claim Construction

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Innova/Pure Water Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To determine the meaning of the claims, courts start by considering the intrinsic evidence. *Id.* at 1313; *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 861 (Fed. Cir. 2004); *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Group, Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001). The intrinsic evidence includes the claims themselves, the specification, and the prosecution history. *Phillips*, 415 F.3d at 1314; *C.R. Bard, Inc.*, 388 F.3d at 861. The general rule—subject to certain specific exceptions discussed *infra*—is that each claim term is construed according to its ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the context of the patent. *Phillips*, 415 F.3d

at 1312–13; *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1368 (Fed. Cir. 2003); *Azure Networks, LLC v. CSR PLC*, 771 F.3d 1336, 1347 (Fed. Cir. 2014) ("There is a heavy presumption that claim terms carry their accustomed meaning in the relevant community at the relevant time.") (vacated on other grounds).

"The claim construction inquiry … begins and ends in all cases with the actual words of the claim." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1248 (Fed. Cir. 1998). "[I]n all aspects of claim construction, 'the name of the game is the claim.'" *Apple Inc. v. Motorola, Inc.*, 757 F.3d 1286, 1298 (Fed. Cir. 2014) (quoting *In re Hiniker Co.*, 150 F.3d 1362, 1369 (Fed. Cir. 1998)). First, a term's context in the asserted claim can be instructive. *Phillips*, 415 F.3d at 1314. Other asserted or unasserted claims can also aid in determining the claim's meaning, because claim terms are typically used consistently throughout the patent. *Id.* Differences among the claim terms can also assist in understanding a term's meaning. *Id*. For example, when a dependent claim adds a limitation to an independent claim, it is presumed that the independent claim does not include the limitation. *Id*. at 1314–15.

"[C]laims 'must be read in view of the specification, of which they are a part.'" *Id*. (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc)). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Id*. (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)); *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002). But, "'[a]lthough the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims.'" *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998) (quoting *Constant v. Advanced Micro-*

Devices, Inc., 848 F.2d 1560, 1571 (Fed. Cir. 1988)); *see also Phillips*, 415 F.3d at 1323. "[I]t is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004).

The prosecution history is another tool to supply the proper context for claim construction because, like the specification, the prosecution history provides evidence of how the U.S. Patent and Trademark Office ("PTO") and the inventor understood the patent. *Phillips*, 415 F.3d at 1317. However, "because the prosecution history represents an ongoing negotiation between the PTO and the applicant, rather than the final product of that negotiation, it often lacks the clarity of the specification and thus is less useful for claim construction purposes." *Id.* at 1318; *see also Athletic Alternatives, Inc. v. Prince Mfg.*, 73 F.3d 1573, 1580 (Fed. Cir. 1996) (ambiguous prosecution history may be "unhelpful as an interpretive resource").

Although extrinsic evidence can also be useful, it is "'less significant than the intrinsic record in determining the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc.*, 388 F.3d at 862). Technical dictionaries and treatises may help a court understand the underlying technology and the manner in which one skilled in the art might use claim terms, but technical dictionaries and treatises may provide definitions that are too broad or may not be indicative of how the term is used in the patent. *Id*. at 1318. Similarly, expert testimony may aid a court in understanding the underlying technology and determining the particular meaning of a term in the pertinent field, but an expert's conclusory, unsupported assertions as to a term's definition are not helpful to a court. *Id*. Extrinsic evidence is "less reliable than the patent

and its prosecution history in determining how to read claim terms." *Id*. The Supreme Court has explained the role of extrinsic evidence in claim construction:

> In some cases, however, the district court will need to look beyond the patent's intrinsic evidence and to consult extrinsic evidence in order to understand, for example, the background science or the meaning of a term in the relevant art during the relevant time period. *See, e.g., Seymour v. Osborne*, 11 Wall. 516, 546 (1871) (a patent may be "so interspersed with technical terms and terms of art that the testimony of scientific witnesses is indispensable to a correct understanding of its meaning"). In cases where those subsidiary facts are in dispute, courts will need to make subsidiary factual findings about that extrinsic evidence. These are the "evidentiary underpinnings" of claim construction that we discussed in *Markman*, and this subsidiary factfinding must be reviewed for clear error on appeal.

Teva Pharm. USA, Inc. v. Sandoz, Inc., 574 U.S. 318, 331–32 (2015).

B. Departing from the Ordinary Meaning of a Claim Term

There are "only two exceptions to [the] general rule" that claim terms are construed according to their plain and ordinary meaning: "1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of the claim term either in the specification or during prosecution."[3] *Golden Bridge Tech., Inc. v. Apple Inc.*, 758 F.3d 1362, 1365 (Fed. Cir. 2014) (quoting *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012)); *see also GE Lighting Solutions, LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) ("[T]he specification and prosecution history only compel departure from the plain meaning in two instances: lexicography and disavowal."). The standards for finding lexicography or disavowal are "exacting." *GE Lighting Solutions*, 750 F.3d at 1309.

To act as his own lexicographer, the patentee must "clearly set forth a definition of the disputed claim term," and "clearly express an intent to define the term." *Id.* (quoting *Thorner*, 669

[3] Some cases have characterized other principles of claim construction as "exceptions" to the general rule, such as the statutory requirement that a means-plus-function term is construed to cover the corresponding structure disclosed in the specification. *See, e.g., CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1367 (Fed. Cir. 2002).

F.3d at 1365); *see also Renishaw*, 158 F.3d at 1249. The patentee's lexicography must appear "with reasonable clarity, deliberateness, and precision." *Renishaw*, 158 F.3d at 1249.

To disavow or disclaim the full scope of a claim term, the patentee's statements in the specification or prosecution history must amount to a "clear and unmistakable" surrender. *Cordis Corp. v. Boston Sci. Corp.*, 561 F.3d 1319, 1329 (Fed. Cir. 2009); *see also Thorner*, 669 F.3d at 1366 ("The patentee may demonstrate intent to deviate from the ordinary and accustomed meaning of a claim term by including in the specification expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope."). "Where an applicant's statements are amenable to multiple reasonable interpretations, they cannot be deemed clear and unmistakable." *3M Innovative Props. Co. v. Tredegar Corp.*, 725 F.3d 1315, 1326 (Fed. Cir. 2013).

C. Previous Constructions of Disputed Terms

C-1. Prior court constructions are entitled to reasoned deference.

The "importance of uniformity in the treatment of a given patent" suggests a level of deference to previous court constructions of disputed claim terms. *See Finisar Corp. v. DirecTV Grp., Inc.*, 523 F.3d 1323, 1329 (Fed. Cir. 2008) (quoting *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 390 (1996)); *Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 574 U.S. 318, 329 (2015) (noting that "prior cases … sometimes will serve as persuasive authority"). While the "doctrine of *stare decisis* does not compel one district court judge to follow the decision of another … previous claim constructions in cases involving the same patent are entitled to substantial weight." *TQP Dev., LLC v. Intuit Inc.*, No. 2:12-CV-180-WCB, 2014 U.S. Dist. LEXIS 84057, at *21–22 (E.D. Tex. June 20, 2014) (Bryson, J.).

C-2. In some instances, a party may be estopped from pursuing a claim construction different from a prior court construction under the equitable doctrine of issue preclusion.

In some instances, previous court construction of a disputed term may trigger issue preclusion and bind a party to a previous construction. *Teva*, 574 U.S. at 329 ("prior cases will sometimes be binding because of issue preclusion") (citing *Markman*, 517 U.S. at 391). "Issue preclusion generally refers to the effect of a prior judgment in foreclosing successive litigation of an issue of fact or law actually litigated and resolved in a valid court determination essential to the prior judgment, whether or not the issue arises on the same or a different claim [for relief]." *New Hampshire v. Maine*, 532 U.S. 742, 748–49 (2001). "Issue preclusion prohibits a party from seeking another determination of the litigated issue in the subsequent action." *Soverain Software LLC v. Victoria's Secret Direct Brand Mgmt., LLC*, 778 F.3d 1311, 1315 (Fed. Cir. 2015) (quoting *State Farm Mut. Auto. Ins. Co. v. Logisticare Sols., LLC*, 751 F.3d 684, 689 (5th Cir. 2014)). Issue preclusion applies only if four conditions are met:

> First, the issue under consideration in a subsequent action must be identical to the issue litigated in a prior action. Second, the issue must have been fully and vigorously litigated in the prior action. Third, the issue must have been necessary to support the judgment in the prior case. Fourth, there must be no special circumstance that would render preclusion inappropriate or unfair.

State Farm, 751 F.3d at 689.

III. AGREED CONSTRUCTIONS

The parties have agreed to constructions set forth in their Joint Claim Construction Chart Pursuant to P.R. 4-5 (Dkt. No. 73). Based on the parties' agreement, the Court hereby adopts the agreed constructions.

IV. CONSTRUCTION OF DISPUTED TERMS

A. "Peripheral Component Interconnect (PCI) bus transaction" and "PCI bus transaction"

Disputed Term[4]	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"Peripheral Component Interconnect (PCI) bus transaction"	information, including at least PCI address, data, byte enable, and command type information, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component	a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component
"PCI bus transaction"		

Because the parties' arguments and proposed constructions with respect to these terms are related, the Court addresses the terms together.

The Parties' Positions

Plaintiff submits: The claimed PCI bus transaction requires some, but not all, information set forth in the PCI Local Bus Specification. Specifically, the claims require "address, data, byte enable, and command information" of the PCI Local Bus Specification but not "the other physical and electrical aspects of the prior art parallel PCI bus." For example, the embodiment of Figure 13 of the '768 Patent lists address, data, byte enable, and command information but omits other prior-art PCI information that is listed in Figure 16. The Figure 13 embodiment also lists information specific to the invented bus, information not found in the prior-art PCI specification. Further, the claimed and described inventions do not necessarily require a PCI bus, meaning that the PCI information related to controlling a parallel PCI bus is not necessary to the invention. In fact, a PCI "transaction" is known in the art to denote PCI address, data, byte enable, and command

[4] A full listing of the text of the claims in which the disputed terms are found is presented in Exhibit B to the parties Joint Claim Construction Chart Pursuant to P.R. 4-5 (Dkt. No. 73-2).

information without including the PCI bus control signals. The claim constructions in the EMC Case addressed a dispute over whether the PCI bus transaction requires a PCI bus and yielded a stipulated construction that Defendants propose here. But the EMC court procedurally foreclosed argument on whether a transaction in accordance with the PCI Local Bus Specification requires more than PCI address, data, byte enable, and command type information. Thus, the issue before the Court here was not litigated in the EMC Case. Dkt. No. 65 at 9–21.

In addition to the claims themselves, Plaintiff cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '768 Patent Figs. 6, 8A–8C, 9–16, 28, 29–31, col.8 ll.24–26, col.8 ll.40–52, col.16 ll.29–31, col.17 l.64 – col.18 l.5, col.21 l.23 – col.22 l.63, col.24 ll.28–52, col.25 ll.13–16; '654 Patent Fig. 16; '140 Patent Fig. 16; *PCI Local Bus Specification* at 9, 21, 95–96, 250,[5] 269, 271–72 (Rev. 2.1 June 1, 1995) (Dkt. Nos. 65-10 – 65-13, 65-10 at 20, 32, 65-12 at 27–28, 65-13 at 39, 41–42); *PCI Local Bus Specification* at 9–10, 21, 93–95, 255,[6] 297, 300–01 (Rev. 2.2 Dec. 18, 1998) (Dkt. Nos. 65-14 – 65-19, 65-14 at 20–21, 32, 65-17 at 19–20, 65-19 at 9, 12–13). **Extrinsic evidence**: Levitt Decl.[7] ¶¶ 32–36, 47–51, 63–97, 112–14 (Dkt. No. 65-6); Levitt Rebuttal Decl.[8] ¶¶ 5–9 (Dkt. No. 65-7); Colwell Decl.[9] ¶¶ 55–58 (Dkt. No. 65-8); Colwell Rebuttal Decl.[10] ¶¶ 6–26 (Dkt. No. 65-9); *PCI-to-PCI Bridge Architecture Specification* 11–13 (Rev. 1.1 Dec. 18, 1998) (Dkt. No. 65-20 at 9–11).

Defendants respond: Plaintiff consistently represented to courts and the PTAB that the recited PCI bus transaction in related patents is a bus transaction defined by the PCI Local Bus Specification. And, as Plaintiff represented to the PTAB in a proceeding on a related patent, a PCI

5 Page 250 of the specification was not submitted in Dkt. Nos. 65-10–65-13.
6 Page 255 of the specification was not submitted in Dkt. Nos. 65-14–65-19.
7 Expert Declaration of Marc. E. Levitt, Ph.D. Regarding Claim Construction (June 3, 2021).
8 Rebuttal Expert Declaration of Marc E. Levitt, Ph.D. Regarding Claim Construction (June 21, 2021).
9 Declaration of Robert P. Colwell, Ph.D. (June 3, 2021).
10 Rebuttal Declaration of Robert P. Colwell, Ph.D. (June 15, 2021).

bus transaction necessarily requires all the bits to complete the transaction, including control bits. Indeed, in the embodiment depicted in Figure 13 of the '768 Patent, PCI control information is embedded in bits BS0–BS3 (citing '768 Patent col.22 ll.31–32). Finally, Plaintiff is estopped from taking the position it now advocates: Specifically, in the *Alcatel Markman*, the Court considered and expressly rejected Plaintiff's position that the PCI bus transaction is a subset of the information set forth in the PCI Local Bus Specification. The *EMC Markman* and *EMC Summary Judgment* reiterated this, and the Massachusetts District Court granted summary judgment based on the claimed PCI bus transaction requiring all the information required by the PCI Local Bus Specification. Dkt. No. 69 at 12–22.

In addition to the claims themselves, Defendants cite the following intrinsic and extrinsic evidence to support their position: **Intrinsic evidence**: '768 Patent Figs. 13–14, 16, col.5 ll.49–55, col.21 l.37 – col.22 l.42; IPR Preliminary Response 8,041,873[11] at 6 (Dkt. No. 69-14 at 12); IPR Institution 8,041,873[12] at 7 (Dkt. No. 69-16 at 8); IPR Hearing Transcript[13] at 35:11–17, 38:5–20, 50:12–16 (Dkt. No. 69-17 at 7, 10, 19); *PCI Local Bus Specification* at 10 (Rev. 2.1 June 1, 1995) (Dkt. Nos. 65-10 – 65-13, 65-10 at 21); *PCI Local Bus Specification* at 10, § 3.7.3, Ch. 5 (Rev. 2.2 Dec. 18, 1998) (Dkt. Nos. 69-18 at 4, 7, 10–45). **Extrinsic evidence**: IPR Preliminary Response RE42,814[14] at 6–10 (Dkt. No. 69-13 at 11–15); IPR Institution RE42,814[15]at 7 (Dkt. No. 69-15 at 8); Colwell Rebuttal Decl. ¶¶ 12–15, 20–26 (Dkt. No. 65-9); Levitt Decl. ¶¶ 14–15, 91 (Dkt. No.

[11] Patent Owner's Preliminary Response, *EMC Corp. v. ACQIS LLC*, IPR2014-01462 (P.T.A.B. Dec. 15, 2014) (U.S. Patent No. 8,041,873).
[12] Decision – Institution of Inter Partes Review, *EMC Corp. v. ACQIS LLC*, IPR2014-01462 (P.T.A.B. Sept. 25, 2014) (U.S. Patent No. 8,041,873).
[13] Hearing Transcript, *EMC Corp. v. ACQIS LLC*, IPR2014-01462 & IPR2014-01469 (P.T.A.B. Dec. 8, 2015) (U.S. Patent Nos. 8,041,873 & RE42,814).
[14] Patent Owner's Preliminary Response, *EMC Corp. v. ACQIS LLC*, IPR2014-01469 (P.T.A.B. Sept. 25, 2014) (U.S. Patent No. RE42,814).
[15] Decision – Institution of Inter Partes Review, *EMC Corp. v. ACQIS LLC*, IPR2014-01469 (P.T.A.B. Mar. 11, 2015) (U.S. Patent No. RE42,814).

65-6); Levitt Dep.[16] at 77:10–24, 82:17 – 83:8, 84:2–9, 105:18 – 106:20 (Dkt. No. 69-12 at 23, 28–30, 33–34).

Plaintiff replies: Collateral estoppel does not apply. While the *Alcatel Markman* stated that "a PCI bus transaction must include all information required by the PCI standard," the Court did not there state what was required by that standard. Nor did the Court state that the standard required more or less than "digital command, address, and data information." In fact, the *Alcatel Markman* rejected that the PCI bus transaction necessarily requires signals or a bus, which are part of the PCI Local Bus Specification.[17] The *EMC Summary Judgment* applied a different understanding of the *Alcatel Markman* construction, and required all of the Specification, including signals and elements pertaining to a physical bus. Further, intrinsic and extrinsic evidence establishes that PCI control and parity signals are not required. Plaintiff's remarks regarding "control" information made to the PTAB reflect "command" information rather than PCI control signals. The '768-Patent Figure 13 embodiment is described as able to incorporate some of the function of some PCI control signals. But this incorporation is expressly optional—the embodiment may incorporate only a subset or none of the PCI control signals required by the PCI Local Bus Specification. And this embodiment does not suggest including parity at all. In fact, the PCI Local Bus Specification states that parity is based on a transaction, not that it is part of a transaction. Dkt. No. 71 at 4–11.

Plaintiff cites further **intrinsic evidence** to support its position: IPR Hearing Transcript at 37:21 – 38:2 (Dkt. No. 69-17 at 9–10).

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[16] Remote Video-Recorded Deposition of Marc E. Levitt, Ph.D. (June 23, 2021).

[17] Plaintiff also argues that requiring every aspect of the PCI Local Bus Specification would be inconsistent with the Court's previous construction of "PCI bus transaction" in *ACQIS LLC v. Appro Int'l, Inc.*, No. 6:09-cv-148, 2011 U.S. Dist. LEXIS 10515 (E.D. Tex. Feb. 3, 2011). The *Alcatel Markman* expressly reconsidered the *Appro* construction. *Alcatel Markman*, 2015 U.S. Dist. LEXIS 48339, at *12 ("The parties agree that the construction in *Appro* should be reconsidered because it did not account for the PCI standard.").

Analysis

The terms "Peripheral Component Interconnect (PCI) bus transaction" and "PCI bus transaction" plainly refer to a transaction with the information required of a "transaction" by the PCI Local Bus Specification. The parties do not dispute this. The issue in dispute appears to be whether a transaction lacking certain control signals is a transaction in accordance with the PCI Local Bus Specification. Indeed, nothing in the Asserted Patents suggests straying from the PCI Local Bus Specification but rather teaches complying with that standard. *See, e.g.*, '768 Patent col.5 ll.49–55 ("In the present invention, PCI control signals are encoded into control bits and the control bits, rather than the control signals that they represent, are transmitted on the interface channel. At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus."); col.18 ll.30–36 ("Control encoder & merge data path unit 1025 encodes PCI control signals … into control bits, merges these encoded control bits and transmits the merged control bits to transmitter 1030**,** which then transmits the control bits on the data lines PD0 to PD3 and control line PCN of the XPBus."), col.21 ll.55–58 ("The bits transmitted on lines PD0 to PD3 represent 32 PCI AD[31::0] signals, 4 PCI C/BE# [3: :0] signals, and part of the function of PCI control signals, such as FRAME#, IRDY#, and TRDY#."), col.22 ll.31–32 ("In one embodiment, BSO and BSl are used to encode the PCI signals FRAME# and IRDY#, respectively.").

The Court declines, however, to rule in claim construction whether a particular set of information qualifies as a transaction under the PCI Local Bus Specification. While the scope of related limitations in related patents has been previously addressed in other cases, the previous determinations do not rise to the level of collateral estoppel regarding the issue here; namely, what set of information qualifies as a transaction under the PCI Local Bus

Specification. The Court understands this as an issue of fact to be considered in the context of an infringement or invalidity analysis rather than an issue of claim construction. Notably, the *Alcatel Markman* determined that a "PCI bus transaction" in related patents does not require a PCI bus. *Alcatel Markman*, 2015 U.S. Dist. LEXIS 48339 ("Defendants have failed to show that a PCI bus 'transaction' necessarily implies the presence of a PCI 'bus.'"). But it did not determine all that is required by the PCI Local Bus Specification to qualify as a transaction. *Id.* at *14–15 ("Although a PCI bus transaction must include all information required by the PCI standard, ACQIS's extrinsic evidence does not clearly define a 'transaction' as digital command, address, and data information."). The *EMC Markman* similarly did not address all of what is required of a PCI bus transaction as defined in the PCI Local Bus Specification, but addressed only the dispute as to whether the PCI bus transaction required a PCI bus and held that "the PCI Local Bus Specification does not define such transactions by the presence of a PCI bus." *EMC Markman,* 2017 U.S. Dist. LEXIS 202160, at *9–11. Finally, the *EMC Summary Judgment* reiterated that "PCI bus transaction" required all the information of the PCI Local Bus Specification, but did not appear to consider Plaintiff's argument that information that "appl[ies] only to the methodology used to convey the PCI bus transaction … are … outside the scope of the PCI bus transaction itself." *EMC Summary Judgment,* 2021 U.S. Dist. LEXIS 55945, at *12. Rather, the court there noted that in the two Markman proceedings at issue, Plaintiff "never attempted to parse the [PCI Local Bus] Specification in order to differentiate the elements that describe the methodology of the PCI bus transaction from those that describe the substance of the transaction." *Id*. at *13. The EMC court ultimately dismissed as untimely Plaintiff's argument that a "transaction" under the PCI Local Bus Specification does not require information used to convey the transaction. *Id*. at *14–15. In this context, where the EMC case involved claims of different

scope in different patents asserted against different technology and where the *EMC Summary Judgment* was premised on the procedural posture rather than whether the PCI Local Bus Specification actually distinguishes between information used to convey a transaction and the transaction itself, collateral estoppel does not apply. *See State Farm Mut. Auto. Ins. Co. v. Logisticare Sols., LLC,* 751 F.3d 684, 689 (5th Cir. 2014).

Ultimately, a PCI bus transaction is a "transaction" as defined by the PCI Local Bus Specification as is known in the art. Whether a particular set of information meets that standard is properly left be determined in the context of infringement or invalidity.

Accordingly, the Court construes these terms as follows:

- "Peripheral Component Interconnect (PCI) bus transaction" means "a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component";
- "PCI bus transaction" means "a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component."

B. "address and data [bits] of a Peripheral Component Interconnect (PCI) bus transaction" and "address bits, data bits, and byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction"

Disputed Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"address and data [bits] of a Peripheral Component Interconnect (PCI) bus transaction" / "address and data bits of a PCI bus transaction"[18]	plain and ordinary meaning	a PCI bus transaction, including all address, data, and control bits

[18] The parties identified the term "address and data bits of a PCI bus transaction" in Exhibit B to their Joint Claim Construction Chart Pursuant to P.R. 4-5 (Dkt. No. 73-2 at 17–30) but not in Exhibit A (Dkt. No. 73-1 at 1–2).

Disputed Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"address bits, data bits, and byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction"		

Because the parties' arguments and proposed constructions with respect to these terms are related, the Court addresses the terms together.

The Parties' Positions

Plaintiff submits: The meanings of these terms are plain without construction. They refer to specific information of the PCI bus transaction. For the reasons provided in the section on "PCI bus transaction," it would be improper to require all PCI control signals. Dkt. No. 65 at 22–23.

Defendants respond: As Plaintiff represented to the PTAB in IPR of a related patent, it is crucial to the invention that all the bits of the PCI standard are transmitted, including control bits. This representation was made concerning a claim term similar to the terms at issue here. Specifically, the IPR remarks were in the context of distinguishing prior art from claims reciting "wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits." In fact, in the dispute with EMC, Plaintiff agreed that "communicate address and data bits of PCI bus transaction" means "communicating a PCI bus transaction, including all address, data, and control bits" (citing *EMC Markman*). Dkt. No. 69 at 22–25.

In addition to the claims themselves, Defendants cite the following intrinsic and extrinsic evidence to support their position: **Intrinsic evidence**: '768 Patent Figs. 13–14, col.21 ll.55–58, col.22 ll.31–32; IPR Response 8,041,873[19] at 8 (Dkt. No. 69-20 at 16); IPR Hearing Transcript at

[19] Patent Owner's Response, *EMC Corp. v. ACQIS LLC*, IPR2014-01462 (P.T.A.B. June 11, 2015) (U.S. Patent No. 8,041,873).

35:11–17, 38:9–20, 39:13–15, 49:13–14 (Dkt. No. 69-17 at 7, 10–11, 18); Lindenstruth Dep.[20] at 145:18 – 146:17, 168:17 – 169:9 (Dkt. No. 69-21 at 4–5, 8–9). **Extrinsic evidence**: IPR Response RE42,814[21] at 8–9 (Dkt. No. 69-19 at 13–14).

Plaintiff replies: In the IPR proceedings, Plaintiff used "control bits" to refer to "command type information," not to control signals. Similarly, in the EMC case, Plaintiff did not agree to a construction that required control signals in a PCI bus transaction. Dkt. No. 71 at 11.

Analysis

The issue in dispute appears to be whether PCI bus transaction "control bits" are necessarily required even when the claim language is expressly directed only to some combination of address bits, data bits, and byte enable information bits. They are not.

The claim language itself provides significant guidance as to the meanings of these terms. For instance, Claim 1 of the '768 Patent provides:

> 1. A computer, comprising:
> an integrated central processing unit, interface controller and Phase-Locked Loop (PLL) clock circuitry in a single chip,
> a Low Voltage Differential Signal (LVDS) channel directly extending from the interface controller ***to convey address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in a serial form***, wherein the first LVDS channel comprises a first unidirectional, differential signal pair to convey data in a first direction and a second unidirectional, differential signal pair to convey data in a second, opposite direction; and
> wherein the PLL clock circuitry generates different clock frequencies, and the interface controller conveys the PCI bus transaction through the LVDS channel based on the different clock frequencies.

'68 Patent col.40 ll.37–53 (emphasis added). Here, the claim language plainly does not require more than "address and data bits of a Peripheral Component Interconnect (PCI) bus transaction."

[20] Deposition of Volker Lindenstruth, *EMC Corp. v. ACQIS LLC*, IPR2014-01462 & IPR2014-01469 (P.T.A.B. Aug. 27, 2015) (U.S. Patent Nos. 8,041,873 & RE42,814)
[21] Patent Owner's Response, *EMC Corp. v. ACQIS LLC*, IPR2014-01469 (P.T.A.B. June 11, 2015) (U.S. Patent No. RE42,814).

The prosecution history of related patents that is of record here does not justify reading Defendants' proposed "all control bits" limitation. Specifically, Defendants rely on the patent owner's arguments made to preserve Claims 54 and 61 of U.S. Patent No. 8,041,873 (the "'873 Patent") in IPR. Those claims provide as follows:

> **54.** A computer module insertable into a coupling site of a console for data communication, comprising: a main circuit board;
> a processing unit coupled to the main circuit board; a main memory coupled to the processing unit;
> a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions ***for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction***; and
> a peripheral bridge directly coupled to the processing unit, the peripheral bridge comprising an interface controller directly coupled to the LVDS channel.
>
> **61.** The computer module of claim **54,** wherein the ***encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits***.

'873 Patent col.43 ll.40–52, col.44 ll.5–7 (emphasis added). Notably, Claim 54 of the '873 Patent requires channels to transmit a "bit stream of Peripheral Component Interconnect (PCI) bus transaction." Thus, the claim requires all the information of a PCI bus transaction. The patent owner's statements during IPR must be interpreted in this context. The exchange between the patent owner and the PTAB judges is instructive:

> JUDGE TIERNEY: I would like to go back to the language of the claims because I think we are reading a few things in and I want to make sure it's okay to do so. Let's start with the ***'873 patent claim 54***. We are talking about encoded serial bit stream. Why do I want to read in the words physical address?
>
> MR. STACY: It is an encoded serial bit stream of peripheral interconnect bus transaction. The Board has already said that the PCI is important, that it's part of it. So you have got to go to the standard. The PCI standard does not allow a virtual address. So you would be reading PCI standard out of claim 54. So in other words, if you put a virtual address in, it's no longer a capital PCI bus transaction. It's something completely different. And that's just straight out of the standard. Dr. Lindenstruth references that several times and we'll talk about that.

> Now, there's something interesting here. They keep going back to this claim differentiation doctrine on claim 61 which showed up in the reply for the first time. You heard it the same time we did, but I would like to the address that.
>
> …
>
> And an important thing here about 61, they said 61 somehow offers claim differentiation. This is something their expert came up with. Well, ***if you look at the standard, there are three types of information included in every PCI transaction. Three types. There's an address, there's data and then there's control. That's straight out of the standard. You have those three things***.
>
> There is a special type of ***PCI transaction known as interrupt acknowledge***. In an interrupt acknowledge, ***the address is zeroed out***. It's null. So if you look at ***claim 54, it says all PCI bus transactions***. That covers everything. What does claim 61 do? Claim 61 narrows it and says this PCI transaction has to have encoded PCI address and data bits. ***Claim 61 actually carves out those interrupt acknowledges***. It carves out a specific type.

IPR Hearing Transcript at 32:5 – 35:24 (emphasis added), Dkt. No. 69-17 at 4–7. The patent owner stated that Claim 54 of the '873 Patent, which involves a PCI bus transaction, requires the address, data, and control bits of a PCI bus transaction and that Claim 61 excludes from the scope of the claim the interrupt acknowledge transaction by requiring non-zero address bits. This does not rise to the level of disclaimer to constrain a list of information items from a PCI bus transaction to require all information of a PCI bus transaction regardless what items are enumerated in the list.

Accordingly, the Court rejects Defendants' proposed construction and determines that these terms have their plain and ordinary meanings without the need for further construction.

C. "encoded," "in [a] serial form," "[in a] serial bit stream," "[in a] serial bit channel[s]," "LVDS channel," and "conveying serially"

Disputed Term[22]	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"encoded"	coded representation of [bits]	

[22] In their Joint Claim Construction Chart Pursuant to P.R. 4-5, the parties identify the disputed terms as "Claim phrases stating that either the recited bits of a PCI bus transaction, as applicable (ACQIS's position), or a PCI bus transaction (Samsung's position), be: …" and further identify specific terms for construction. Dkt. No. 73-1 at 2–3; Dkt. No. 73-2 at 30–43. The parties further preface "in [a] serial form," "[in a] serial bit stream," "[in a] serial bit channel[s]," and "LVDS channel" with "conveyed / transmitted / communicated serially, i.e.," in the chart. *Id*. Other

Disputed Term[22]	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"in [a] serial form"	one bit at a time per bit-based line	a PCI bus transaction that has been serialized from a parallel form
"[in a] serial bit stream"	[in] a flow of information in which units of information are transferred serially	
"[in a] serial bit channel[s]"	[in] a flow of information in which units of information are transferred serially	
"LVDS channel"[23]	no construction necessary	
"conveying serially"	conveying one bit at a time per bit-based line	

Because the parties' arguments and proposed constructions with respect to these terms are related, the Court addresses the terms together.

The Parties' Positions

Plaintiff submits: As these terms are customarily used in the art and as used in the Asserted Patents, they are not limited to require a parallel-to-serial conversion of a parallel PCI bus transaction. The Asserted Patents describe embodiments in which a chip is directly connected to a channel for conveying encoded bits, without the need for a parallel-to-serial conversion. Embodiments which include a parallel-to-serial conversion describe the conversion as distinct from encoding. Similarly, the "serial" terms are directed to how the bits are conveyed/transmitted without regard to any conversion of a PCI bus transaction. The *Alcatel Markman* expressly rejected a parallel-to-serial conversion in construing "encoded PCI bus transaction." And while the *EMC*

than the proposed constructions for the particular phrases listed here, Plaintiff contends that the "remaining portions of [the terms in dispute] do not require construction." Dkt. No. 73-1 at 2–3.

[23] The term identified in the full-text listing of the claims in the parties' P.R. 4-5(d) chart is "Low Voltage Differential Signal (LVDS) channel." Dkt. No. 73-2 at 30–43.

Markman construed "encoded" terms to require a parallel-to-serial conversion, it did so based on an IPR disclaimer that is not applicable here and for patents with different claims and disclosures than the Asserted Patents. Dkt. No. 65 at 23–29.

In addition to the claims themselves, Plaintiff cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '768 Patent Figs. 8A–8B, 10, col.5 ll.50–65, col.15 l.57 – col.16 l.36, col.17 ll.29–46, col.17 ll.56–64, col.18 l.63 – col.19 l.17, col.25 ll.3–7; U.S. Patent No. 8,041,873 col.5 ll.34–48; **Extrinsic evidence**: *The IEEE Standard Dictionary of Electrical and Electronic Terms* at 355, 970–71 (6th ed. 1996), "encode," "serial," and "serial transmission" (Dkt. No. 65-21 at 5, 9); Levitt Decl. ¶¶ 36, 110, 112–17, 119 (Dkt. No. 65-6).

Defendants respond: "The specifications unambiguously disclose that to use [the disclosed serial] interface, the PCI bus transactions (which are in parallel form) are encoded and converted to serial form and are then transmitted over the interface channel." There is no description in the Asserted Patent of a PCI bus transaction over the serial channel that does not involve a parallel-to-serial conversion. Further, during IPR of U.S. Patent No. 8,041,873, Plaintiff represented to the PTAB that the invention necessarily required conversion of a PCI bus transaction from parallel to serial form. As set forth in the *EMC Markman*, these representations constitute disclaimer. Dkt. No. 69 at 25–30.

In addition to the claims themselves, Defendants cite the following intrinsic and extrinsic evidence to support their position: **Intrinsic evidence**: '768 Patent Figs. 7, 8, 10–11, 29–30, col.3 ll.19–22, col.5 ll.49–55, col.6 ll.41–65, col.16 ll.22–27, col.17 ll.59–64, col.18 l.11 – col.19 l.17, col.23 ll.46–56; IPR Hearing Transcript at 32:2–4, 34:14–18, 39:21 – 40:2, 46:14 – 47:18, 51:11–12, 61:6–23 (Dkt. No. 69-17 at 4, 5, 11–12, 15–16, 20, 23). **Extrinsic evidence**: Levitt Dep. at 68:3–24 (Dkt. No. 69-12 at 20); Colwell Rebuttal Decl. ¶¶ 36–39 (Dkt. No. 65-9).

Plaintiff replies: The presence of the direct-connection embodiments of Figures 8A and 8B in the '768 Patent and the lack of those embodiments in U.S. Patent No. 8,041,873 mean that the claims of the Asserted Patents should not be limited to require parallel-to-serial conversion through inventor lexicography or disclaimer. Dkt. No. 71 at 11–12.

Analysis

The issues in dispute distill to whether these terms necessarily require a parallel-to-serial conversion of a PCI bus transaction. They do not.

The claim language at issue, which is directed to a PCI bus transaction that is encoded or is conveyed, transmitted, or communicated serially, is not necessarily a transaction that has been converted from parallel to serial form. Such a conversion is not specified in the claims and Defendants' have not met the exacting standard to establish disclaimer. Specifically, Defendants have not identified anything in the Asserted Patents themselves that rises to lexicography or disclaimer such as to restrict all encoded or serially transmitted PCI bus transactions to transactions that have been serialized from a parallel form. Indeed, the embodiments in which a chip/controller is directly connected to a serial channel, without an intervening parallel bus, suggest that the transaction may originate in serial form. *See, e.g.*, '768 Patent Figs. 8A–8B. Plaintiff's IPR characterizations of the invention of U.S. Patent No. 8,041,873 (the "'873 Patent") do not establish that the claims of the Asserted Patents necessarily require a PCI bus transaction that originated in parallel form. The remarks regarding the "invention" of a related patent that has a different disclosure and claim set than that Asserted Patents do not rise to the level of disclaimer for the Asserted Patents. For example, the '873 Patent does not include anything equivalent to Figures 8A and 8B of the '768 Patent. Similarly, some of the claims of the Asserted Patents do not require a PCI bus transaction at all. *See, e.g.*, '797 Patent Claims 27, 30, 33; '768 Patent Claim 36. In this

context, even if the invention of the '873 Patent is somehow limited to a PCI bus transaction that has been converted from parallel to serial, it would be improper to so limit the claims of the Asserted Patents.

Accordingly, the Court rejects Defendants' proposed construction, determines that "LVDS channel" has its plain and ordinary meaning without the need for further construction, and construes the remaining terms as follows:

- "encoded" means "coded representation of [bits]";
- "in [a] serial form" means "one bit at a time per bit-based line";
- "[in a] serial bit stream" means "[in] a flow of information in which units of information are transferred serially";
- "[in a] serial bit channel[s]" means "[in] a flow of information in which units of information are transferred serially";
- "conveying serially" means "conveying one bit at a time per bit-based line."

D. "data transfer signal"

Disputed Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"data transfer signal"	plain and ordinary meaning, alternatively, • signal that transfers data	the FRAME# control signal that initiates and terminates the PCI bus transaction

The Parties' Positions

Plaintiff submits: The meaning of "data transfer signal" is plain in the context of the surrounding claim language and the description of the invention—it refers to "a clock signal that transfers data." In fact, the FRAME# control signal Defendants' propose is incompatible with the claimed LVDS channel. Dkt. No. 65 at 29–31.

In addition to the claims themselves, Plaintiff cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '768 Patent Figs. 13–15, col.18 ll.52–55, col.21 ll.37 – col.22 l.63. **Extrinsic evidence**: Levitt Decl. ¶¶ 132–35 (Dkt. No. 65-6).

Defendants respond: The term "data transfer signal" does not have a customary meaning in the art and thus is a term coined for the '768 Patent. As claimed, the "data transfer signal" is used to convey a PCI bus transaction through the LVDS channel and the "the only signal known to a POSITA that is used to initiate a PCI bus transaction is the FRAME# signal." Dkt. No. 69 at 30–31.

In addition to the claims themselves, Defendants cite the following **extrinsic evidence** to support their position: Colwell Decl. ¶¶ 65–69 (Dkt. No. 65-8).

Plaintiff replies: There is nothing in the intrinsic record that justifies Defendants' proposed construction. Dkt. No. 71 at 12–13.

Analysis

The issue in dispute is whether the "data transfer signal" is necessarily the FRAME# control signal of the PCI Local Bus Specification. It is not.

The claims provide significant context that informs the meaning of "data transfer signal." For example, Claim 13 of the '768 Patent provides:

> 13. A computer, comprising:
> an integrated central processing unit and interface controller in a single chip;
> a first Low Voltage Differential Signal (LVDS) channel directly extending from the interface controller to convey address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in a serial bit stream, wherein the first LVDS channel comprises first unidirectional, multiple, differential signal pairs to convey data in a first direction and second unidirectional, multiple, differential signal pairs to convey data in a second, opposite direction; and
> a system memory directly coupled to the integrated central processing unit and interface controller.

> 17. The computer of claim 13, wherein the interface controller couples to Phase-Locked Loop (PLL) clock circuitry, and wherein ***the interface controller generates a data transfer signal to convey the PCI bus transaction through the LVDS channel based on one of the different clock frequencies generated by the PLL clock circuitry***.

'768 Patent col.42 ll.9–41 (emphasis added). Under a plain reading, the surrounding language of the claim sufficiently defines the data transfer signal. It is a signal that is generated by the interface controller based on a clock frequency generated by the PLL clock circuitry. As Plaintiff contends, this plain reading comports with the description of the embodiment of Figure 10, in which a PLL is used to generate a signal that drives the serial bus. '768 Patent col.18 ll.50–62.

Accordingly, the Court rejects Defendants' proposed construction and determines that this term has its plain and ordinary meaning without the need for further construction.

E. "Universal Serial Bus (USB) protocol," "Universal Serial Bus (USB) protocol data," and "Universal Serial Bus (USB) protocol information"

Disputed Term[24]	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"USB"		[data/information conveyed according to] the protocols defined in the Universal Serial Bus Specification Revision 2.0 and the prior versions of this standard
"Universal Serial Bus (USB) protocol"	USB data payload	
"Universal Serial Bus (USB) protocol data"		
"Universal Serial Bus (USB) protocol information"	information described in the USB specification	

Because the parties' arguments and proposed constructions with respect to these terms are related, the Court addresses the terms together.

[24] The parties also identified "USB" alone as a term in dispute but did not list this term apart from the composite phrases in their full-text claim-listing in their P.R. 4-5(d) chart. Dkt. No. 73-1 at 3, Dkt. No. 73-2 at 44–52.

The Parties' Positions

Plaintiff submits: While these terms invoke the USB protocol, they "do not require every aspect of the USB specifications." Notably, the claims at issue are directed to maintaining software compatibility with USB, but without requiring "the physical and electrical implementation of the Universal Serial Bus." Indeed, many of the claims expressly diverge from the full USB specification. For example, Claim 24 of the '750 Patent (among others) is directed to full-duplex communication whereas the USB specifications existing at the time of invention were directed to half-duplex communication. Ultimately, as used in the Asserted Patents, "Universal Serial Bus (USB) protocol [data]" refers to the USB "data payload" while the broader term "Universal Serial Bus (USB) protocol information" refers to "any information described in the USB specifications." Dkt. No. 65 at 31–34.

In addition to the claims themselves, Plaintiff cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '768 Patent col.5 ll.47–49, col.6 ll.1–3, col.12 ll.16–18, col.18 ll.59–62, col.21 l.37 – col.22 l.42, col.25 ll.8–12; *Universal Serial Bus Specification* at 1, § 5.3.2, § 8.4.3, (Rev. 1.0 Jan. 15, 1996) (Dkt. Nos. 65-22 – 65-24, 65-22 at 2, 65-23 at 2–4, 65-24 at 19); *Universal Serial Bus Specification* at i, § 5.3.2, § 8.4.4 (Rev. 2.0 Apr. 27, 2000) (Dkt. Nos. 65-25 – 65-28, 65-25 at 2, 65-26 at 5–7, 65-27 at 30–31, 65-28 at 2–10). **Extrinsic evidence**: Levitt Decl. ¶¶ 35, 38, 139–44 (Dkt. No. 65-6); Colwell Decl. ¶ 63 (Dkt. No. 65-8).

Defendants respond: The USB protocol of the Asserted Patents is defined by the USB specifications in existence at the time of invention (circa 2000). These do not include a full-duplex USB version, which was not introduced until 2008. Further, there is no reason to require only a

subset of the USB protocol set forth in the USB specifications, which requires more than just data. Dkt. No. 69 at 31–34.

In addition to the claims themselves, Defendants cite the following intrinsic and extrinsic evidence to support their position: **Intrinsic evidence**: '768 Patent col.12 ll.16–17; *Universal Serial Bus Specification* at 85–118, §§ 4.4, 8.2, 8.3.1 (Rev. 2.0 Apr. 27, 2000) Dkt. No. 69-23 at 4–5, 7–40, 43–45). **Extrinsic evidence**: Colwell Decl. ¶¶ 61–62 (Dkt. No. 65-8); Colwell Rebuttal Decl. ¶¶ 43–46 (Dkt. No. 65-9); Levitt Dep. at 42:20 – 43:4, 43:9–18, 49:7 – 50:5 (Dkt. No. 69-12 at 9–10, 13–14); *Universal Serial Bus 3.0 Specification* at ii, § 4.3.1 (Rev. 1.0 Nov. 12, 2008) (Dkt. No. 69-21 at 3, 6).

Plaintiff replies: In the context of the surrounding claim language and the description of the inventions, which refer to USB data and information, these terms refer to a subset of the USB protocol. Dkt. No. 71 at 13.

Analysis

The issue in dispute distills to whether the USB protocol of the claims is the USB protocol known at the priority date of the Asserted Patents. It is.

The claims provide significant context that informs the meanings of these terms. For instance, Claim 36 of the '768 Patent provides:

> **'768 Patent Claim 36.** A computer, comprising:
> an integrated central processing unit and graphics sub- system in a single chip;
> a first Low Voltage Differential Signal (LVDS) channel directly extending from the integrated central processing unit and graphics subsystem, wherein the first LVDS channel comprises a first unidirectional, differential signal pair to convey data in a first direction and a second unidirectional, differential signal pair to convey data in a second, opposite direction, wherein the first LVDS channel ***conveys data using a Universal Serial Bus (USB) protocol***;
> a system memory directly coupled to the integrated central processing unit and graphics subsystem; and
> a graphics memory directly coupled to the integrated central processing unit and graphics subsystem.

'768 Patent col.44 l.58 – col.45 l.6 (emphasis added). Under a plain reading, Claim 36 of the '768 Patent requires a channel that "conveys data using a Universal Serial Bus (USB) protocol." Plaintiff has not identified anything in the intrinsic record that justifies straying from the plain meaning of this term to cover a channel that conveys data using some other protocol, or a subset of the USB protocol. And the term "Universal Serial Bus (USB) protocol" must be interpreted as of the priority date. Claim 18 of the '140 Patent provides a slightly different context:

> **'140 Patent Claim 18**. A method of improving performance of a computer, comprising:
> obtaining an integrated Central Processing Unit (CPU) with a graphics controller in a single chip;
> connecting a Differential Signal channel directly to the integrated CPU and graphics controller to output video data;
> providing a connector for the computer for connection to a console;
> providing a first Low Voltage Differential Signal (LVDS) channel to couple to the connector, the first LVDS channel comprising two unidirectional, serial bit channels that transmit data in opposite directions; and
> ***conveying Universal Serial Bus (USB) protocol information through the first LVDS channel***.

'140 Patent col.23 ll.6–20 (emphasis added). A plain reading of this claim does not restrict the conveyance to one using a USB protocol but rather requires conveyance of USB protocol information. While the information is necessarily in accordance with the USB standard known as of the priority data, the conveyance is not. The term "Universal Serial Bus (USB) protocol data" is found in a similar context. For instance, Claim 33 of the '797 Patent provides:

> **33.** A method of improving external peripheral data performance within a computer, comprising:
> coupling an integrated Central Processing Unit (CPU) and graphics controller chip to a connector,
> conveying a first Low Voltage Differential Signal (LVDS) channel through the connector comprising two unidirectional, serial channels that transmit data in opposite directions;
> ***conveying Universal Serial Bus (USB) protocol data*** from the integrated CPU and graphics controller chip, ***over the first LVDS channel*** for external USB protocol data communication.

'797 Patent col.42 ll.5–15 (emphasis added). While the data that is conveyed is necessarily in accordance with the USB standard known as of the priority data, the conveyance is not.

Accordingly, the Court determines that "USB" alone does not require construction and construes the remaining terms as follows:

- "Universal Serial Bus (USB) protocol" means "the protocols defined in the Universal Serial Bus Specification Revision 2.0 and the prior versions of this standard,"
- "Universal Serial Bus (USB) protocol data" means "data in accordance with the protocols defined in the Universal Serial Bus Specification Revision 2.0 and the prior versions of this standard,"
- "Universal Serial Bus (USB) protocol information" means "information in accordance with the protocols defined in the Universal Serial Bus Specification Revision 2.0 and the prior versions of this standard"

F. "console"

Disputed Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"console"	a device or enclosure, housing one or more coupling sites, that connects components of a computer system	plain and ordinary meaning alternatively, • a chassis that connects several components of the computer system

The Parties' Positions

Plaintiff submits: As described in the '768 Patent, a "console" is an enclosure that is capable of housing coupling sites each comprising a connector. This may be, for example, a "computing device with a motherboard, and need not be a mere chassis alone." Dkt. No. 65 at 35.

In addition to the claims themselves, Plaintiff cites the following **intrinsic evidence** to support its position: '768 Patent, at [57] Abstract, col.4 ll.31–35, col.4 ll.46–50, col.10 l.57 – col.11 l.2.

Defendants respond: In the *Alcatel Markman*, the Court construed "console" as "a chassis that connects several components of the computer system." This is a correct construction for "console" in the Asserted Patents. Notably, there is no suggestion in the Asserted Patents that a console may be a "computing device on its own." Dkt. No. 69 at 34–35.

In addition to the claims themselves, Defendants cite the following intrinsic and extrinsic evidence to support their position: **Intrinsic evidence**: '768 Patent, at [57] Abstract, col.4 ll.49–50, col.10 ll.57–58. **Extrinsic evidence**: Levitt Dep. at 55:5–10 (Dkt. No. 69-12 at 17).

Plaintiff replies: The construction set forth in the *Alcatel Markman* involved multi-module claims and is not appropriate for the different claims here. Dkt. No. 71 at 13.

Analysis

The issue in dispute appears to be whether a console may be a device. It may. At the hearing, the parties agreed to the construction set forth below.

The "console" of the Asserted Patents is defined primarily by its ability to house coupling sites that are used to connect components of a computer system. For example, the '768 Patent provides:

> In a specific embodiment, the present invention provides a computer system for multi-processing purposes. The computer system ***has a console comprising a first coupling site and a second coupling site, e.g., computer module bay. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site.*** The system also has a plurality of computer modules, where each of the computer modules is coupled to one of the connectors. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, and a mass storage device coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system.

> In an alternative specific embodiment, the present invention provides a multi-processing computer system. ***The system has a console comprising a first coupling site and a second coupling site. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site***.

'768 Patent col.4 ll.30–50 (emphasis added). The patent provides another exemplary console:

> The shared peripheral ***console has a chassis and a motherboard that connects the following devices***:
>
> 1) Input means, e.g. keyboard and mouse,
>
> 2) Display means, e.g. RGB monitor,
>
> 3) Add-on means, e.g. PCI add-on slots,
>
> 4) Two Computer Module Bays (CMB) with connectors to two ACMs,
>
> 5) A serial communication Hub controller that interfaces to serial communication controller of both ACMs,
>
> 6) Shared storage subsystem, e.g. Floppy drive, CDROM drive, DVD drive, or 2nd Hard Drive,
>
> 7) Communication device, e.g. modem,
>
> 8) Power supply, and others.

'768 Patent col.10 l.57 – col.11 l.2 (emphasis added).

Accordingly, the Court construes this term as follows:

- "console" means "a device, chassis, or enclosure, housing one or more coupling sites, that connects components of a computer system."

V. CONCLUSION

The Court adopts the constructions above for the disputed and agreed terms of the Asserted Patents. Furthermore, the parties should ensure that all testimony that relates to the terms addressed in this Order is constrained by the Court's reasoning. However, in the presence of the jury the parties should not expressly or implicitly refer to each other's claim construction positions and should not expressly refer to any portion of this Order that is not an actual construction adopted

by the Court. The references to the claim construction process should be limited to informing the jury of the constructions adopted by the Court.

SIGNED this 26th day of September, 2021.

ROY S. PAYNE
UNITED STATES MAGISTRATE JUDGE